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## PATENT ABSTRACTS OF JAPAN

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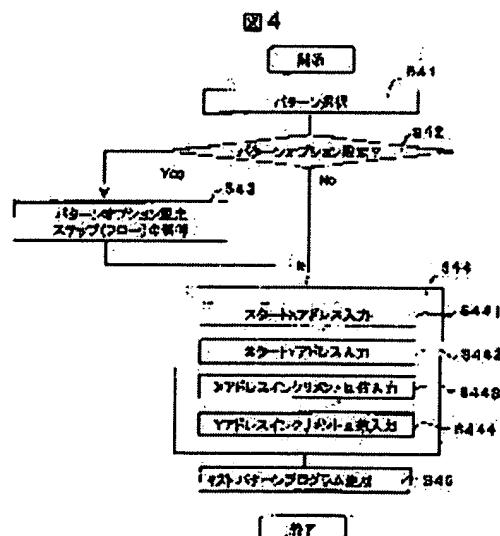
KAWAKAMI MASAMI

### (54) AUTOMATIC GENERATING METHOD FOR LSI TEST PATTERN PROGRAM, ITS DEVICE, AND LSI TEST METHOD

#### (57)Abstract:

**PROBLEM TO BE SOLVED:** To provide an automatic generating method for a LSI test pattern program which can generate automatically a test pattern program easily when capacity, the number of I/O, and the like are changed, its device, and a LSI test method, in a semiconductor memory such as a DRAM, a SRAM, a FLASH or the like.

**SOLUTION:** This method has a process provided with a write-in signal required for a semiconductor memory and plural test conditions in which a two-dimensional scanning direction for generating a test pattern is described as a database, a process in which a provided table of the plural test conditions is displayed and a test condition is selected for plural steps, a process in which a two-dimensional scanning region for generating a test pattern is set, and a process in which a test pattern program for a semiconductor memory is generated based on test conditions for the selected plural steps and the set two-dimensional scanning region.



## LEGAL STATUS

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**CLAIMS**

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**[Claim(s)]**

[Claim 1] The preparation process which prepares two or more test conditions which described the scanning direction for [ which is needed for the semiconductor memory of the class specified ] generating a test pattern and this test pattern at least as a database, The test-condition selection process which chooses the test condition suitable for the semiconductor memory of the class as which the list of said two or more test conditions prepared in this preparation process is displayed, and a test objective is specified about two or more steps, The scan field setting-out process in which the scan field for generating the test pattern suitable for the semiconductor memory of the class as which said test objective is specified is set up, The program generation process which generates the test pattern program over the semiconductor memory of the class as which said test objective is specified based on the test condition about two or more steps chosen in said test-condition selection process, and the scan field set up in said scan field setting-out process The LSI test pattern program automatic generation method characterized by having.

[Claim 2] The LSI test pattern program automatic generation method according to claim 1 characterized by having the option setting-out process in which a pattern option is set up before said program generation process.

[Claim 3] The LSI test pattern program automatic generation method according to claim 1 characterized by displaying on a screen the CAD information on the semiconductor memory of a class that said test objective is specified, in said scan field setting-out process, and setting up said scan field on this screen.

[Claim 4] The LSI test pattern program automatic generation method according to claim 3 characterized by having the capacity selection process which chooses the capacity of the semiconductor memory of the class as which said test objective is specified in said scan field setting-out process, and controlling presenting of said CAD information based on this selected capacity.

[Claim 5] The LSI test pattern program automatic generation method according to claim 1 or 2 which prepares said test condition about the semiconductor memory of two or more classes as a database, and is characterized by generating a test pattern program to the semiconductor memory of two or more classes in said program generation process in said preparation process.

[Claim 6] In an LSI test pattern program automatic generation method according to claim 1 Furthermore, the signal train acquired for every step based on the test pattern program generated in said program generation process is written in the semiconductor memory of the class as which said test objective is specified. As compared with a criterion, pass/fail signal train is acquired about the test result for every step obtained in the trial process which reads the test result for said every step, and this trial process. The LSI test approach which carries out address translation of this and is characterized by having the fail bit map creation process in which the fail bit map for every step is made to create and memorize.

[Claim 7] The storage which stores two or more test conditions which described the scanning direction for [ which is needed for the semiconductor memory of the class specified ] generating a test pattern and this test pattern at least as a database, The test-condition selection section which chooses the test

condition suitable for the semiconductor memory of the class as which the list of said two or more test conditions stored in this storage is displayed, and a test objective is specified about two or more steps, The scan field setting-out section which sets up the scan field for generating the test pattern suitable for the semiconductor memory of the class as which said test objective is specified, The program generation section which generates the test pattern program over the semiconductor memory of the class as which said test objective is specified based on the test condition about two or more steps chosen in said test-condition selection section, and the scan field set up in said scan field setting-out section LSI test pattern program automatic generation equipment characterized by having.

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**DETAILED DESCRIPTION**

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**[Detailed Description of the Invention]****[0001]**

[Field of the Invention] This invention relates to the LSI test approach at the LSI test pattern program automatic generation method used for the electric functional test equipment (circuit tester) to semiconductor devices, such as LSI, and its equipment list.

**[0002]**

[Description of the Prior Art] As a conventional technique about LSI test pattern program automatic generation, it is known in JP,11-83959,A. The test pattern generation section which generates the test pattern which detects failure of the arbitration in circuit information on this conventional technique, The circuit information cutout for deleting the circuit information which receives effect in the test pattern generated by the test pattern generation section, The test pattern generator equipped with the test pattern merge section for merging the test pattern which the test pattern generation section generated to the circuit information after being deleted with the circuit information before being deleted by the circuit information cutout is indicated.

**[0003]**

[Problem(s) to be Solved by the Invention] However, it was not taken into consideration about the method of generation of a test pattern program when capacity, the number of I/O, etc. are changed into the above-mentioned conventional technique in semiconductor memory, such as DRAM and SRAM.

[0004] That the above-mentioned technical problem should be solved, the object of this invention is to provide with the LSI test approach the LSI test pattern program automatic generation method which enabled it to generate a test pattern program automatically easily, and its equipment list, when capacity, the number of I/O, etc. are changed in semiconductor memory, such as DRAM, SRAM, and FLASH.

**[0005]**

[Means for Solving the Problem] The preparation process which prepares two or more test conditions which described-dimensional [ 1 ] or the two-dimensional scanning direction for [ which needs this invention for the semiconductor memory of the class specified in order to attain the above-mentioned object ] generating a test pattern and this test pattern at least as a database, The test-condition selection process which chooses the test condition suitable for the semiconductor memory of the class as which the list of said two or more test conditions prepared in this preparation process is displayed, and a test objective is specified about two or more steps, The scan field setting-out process in which-dimensional [ 1 ] or the two-dimensional scan field for generating the test pattern suitable for the semiconductor memory of the class as which said test objective is specified is set up, The test pattern program over the semiconductor memory of the class as which said test objective is specified based on-dimensional [ 1 ] or the two-dimensional scan field set up in the test condition about two or more steps chosen in said test-condition selection process, and said scan field setting-out process It is the LSI test pattern program automatic generation method characterized by having the program generation process to generate.

[0006] Moreover, this invention is characterized by having the option setting-out process in which a pattern option is set up before the program generation process in said LSI test pattern program automatic

generation method. Moreover, in the scan field setting-out process in said LSI test pattern program automatic generation method, this invention displays on a screen the CAD information on the semiconductor memory of a class that said test objective is specified, and is characterized by setting up said-dimensional [ 1 ] or two-dimensional scan field on this screen. Moreover, in the scan field setting-out process in said LSI test pattern program automatic generation method, this invention has the capacity selection process which chooses the capacity of the semiconductor memory of the class as which said test objective is specified, and is characterized by controlling presenting of said CAD information based on this selected capacity. Moreover, in the preparation process in said LSI test pattern program automatic generation method, this invention prepares said test condition about the semiconductor memory of two or more classes as a database, and is characterized by generating a test pattern program to the semiconductor memory of two or more classes in said program generation process.

[0007] Moreover, this invention is set to said LSI test pattern program automatic generation method. Furthermore, the signal train acquired for every step based on the test pattern program generated in said program generation process is written in the semiconductor memory of the class as which said test objective is specified. As compared with a criterion, pass/fail signal train is acquired about the test result for every step obtained in the trial process which reads the test result for said every step, and this trial process. It is the LSI test approach which carries out address translation of this and is characterized by having the fail bit map creation process in which the fail bit map for every step is made to create and memorize.

[0008] Moreover, the storage which stores two or more test conditions which described-dimensional [ 1 ] or the two-dimensional scanning direction for [ which needs this invention for the semiconductor memory of the class specified ] generating a test pattern and this test pattern at least as a database, The test-condition selection section which chooses the test condition suitable for the semiconductor memory of the class as which the list of said two or more test conditions stored in this storage is displayed, and a test objective is specified about two or more steps (means), The scan field setting-out section which sets up-dimensional [ 1 ] or the two-dimensional scan field for generating the test pattern suitable for the semiconductor memory of the class as which said test objective is specified (means), The test pattern program over the semiconductor memory of the class as which said test objective is specified based on-dimensional [ 1 ] or the two-dimensional scan field set up in the test condition about two or more steps chosen in said test-condition selection section, and said scan field setting-out section It is LSI test pattern program automatic generation equipment characterized by having the program generation section (means) to generate.

[0009]

[Embodiment of the Invention] The gestalt of operation of the LSI test pattern program automatic generation equipment concerning this invention and its approach is explained using a drawing. First, the outline configuration of the LSI test pattern program automatic generation equipment concerning this invention is explained using drawing 1. Namely, LSI test pattern program automatic generation equipment The complicated configuration which had the selected (setting out) rectangle or irregularity so that it might be suitable for classes, such as semiconductor memory, for example, DRAM and SRAM, and FLASH, the capacity of those, etc. (the case of one dimension is sufficient.) EWS1 which is made to scan the inside of the field which it has with various scanning modes, and generates various test patterns (engineering workstation), The storage 2 which stored the test-condition (write-in scan conditions are also included) list for generating the various test patterns to need for every class of semiconductor memory fundamentally etc. as a database, For example, DUT3 which is the semiconductor memory which has various gestalten from which classes, such as DRAM, SRAM, and FLASH, and the capacity of those differ (Device Under Test), The circuit tester 4 which writes the various test patterns generated by the above EWS 1 in DUT3, and reads a test result ("1" a signal train or "0" signal train) from DUT3, The input unit 5 which chooses and inputs various test conditions etc., The output units 6, such as a display which outputs and displays the CAD information on DUT3 which is the above-mentioned test objective (design information), the test pattern scan field for choosing, the

information about various test patterns, etc., are connected in a network 7, and it is constituted. In addition, the test condition for generating beforehand the various test patterns needed using CAD information etc. for every class of semiconductor memory is chosen as the above-mentioned storage 2, and the test-condition chart for every class of semiconductor memory as shown in drawing 3 is stored in it as a database. Therefore, the range which chooses a test condition can be narrowed.

[0010] Moreover, the information (a class, capacity, the number of I/O, etc.) about DUT3 which it is going to examine by the circuit tester 4 is decoded by the above-mentioned storage 2 based on the part number and lot number which are directly read in DUT3 which it is going to examine, and is stored in it. Moreover, the CAD information about the semiconductor memory of various gestalten is inputted and stored in storage 2 through the network 7 from the CAD system. Therefore, EWS1 or a circuit tester 4 can retrieve and acquire the CAD information (design information) from storage 2 based on the information about DUT which it is going to examine. Moreover, you may perform making the inside of the selected (setting out) rectangle or a field scan with various scanning modes, and generating various test patterns in CPU or the circuit in not EWS1 but the circuit tester 4 so that it may be suitable for a class, its capacity, the number of I/O, etc. of semiconductor memory. That is because the circuit tester 4 is connected to storage 2, the input unit 5, and the display 6 that is an output unit through the network 7.

[0011] Next, the various test patterns concerning this invention are explained using drawing 2 and drawing 3. The various write-in test patterns in the case of DRAM or SRAM are shown in drawing 2. the inside of the field where the various write-in test patterns shown in drawing 2 (a) were chosen (setting out) -- setting -- "1" -- a scan is repeated for a signal in the direction of +X (the direction of forward X) (X++), and, moreover, a step is repeated in the direction (the direction of forward Y) of +Y (/Y++). the inside of the field where the test pattern shown in drawing 2 (b) was chosen (setting out) -- setting -- "0" -- a scan is repeated for a signal in the direction of +X (X++), and, moreover, a step is repeated in the direction of +Y (/Y++). the inside of the field where the test pattern shown in drawing 2 R> 2 (c) was chosen (setting out) -- setting -- "1" -- a scan is repeated for a signal in the direction (the direction of forward Y) of +Y (Y++), and, moreover, a step is repeated in the direction of -X (the direction of negative X) (/X --). the inside of the field where the test pattern shown in drawing 2 (d) was chosen (setting out) -- setting -- "0" -- a scan is repeated for a signal in the direction of +Y (Y++), and, moreover, a step is repeated in the direction of -X (/X --). the inside of the field where the test pattern shown in drawing 2 (e) was chosen (setting out) -- setting -- "1" -- a scan is repeated for a signal in the direction of -X (X --), and, moreover, a step is repeated in the direction of +Y (/Y++). [ in the field chosen as a test pattern outside this (setting out) ] "0" -- what repeats a scan for a signal in the direction of -X (X --), and moreover repeats a step in the direction of +Y (/Y++) -- "1" -- what repeats a scan for a signal in the direction of -Y, and moreover repeats a step in the direction of -X -- [ moreover, ] "0" -- what repeats a scan for a signal in the direction of -Y, and moreover repeats a step in the direction of -X -- [ moreover, ] "1" -- the thing which repeats a scan for a signal in the direction of -Y, and moreover repeats a step in the direction of +X, and "0" -- the thing which repeats a scan for a signal in the direction of -Y, and moreover repeats a step in the direction of +X and the thing scanned every other line, the thing scanned every other pit can be considered. [ moreover, ]

[0012] The test-condition database which contains in drawing 3 the scanning-type (scanning mode) for [ which was memorized by storage 2 ] generating the test pattern of every class (form) of semiconductor memory fundamentally is shown. That is, as a test-condition database, it consists of a pattern name, the write-in signal / read-out signal at that time, and a scanning direction. A pattern (PTN) 01 writes in "1", reads "1", repeats a scan in the direction of + of X as a scanning-type (X++), and, moreover, repeats a step in the direction of + of Y (/Y++). A pattern (PTN) 02 writes in "0", reads "0", repeats a scan in the direction of + of X as a scanning-type (X++), and, moreover, repeats a step in the direction of + of Y (/Y++). A pattern (PTN) 03 writes in "0", reads "1", repeats a scan in the direction of + of X as a scanning-type (X++), and, moreover, repeats a step in the direction of + of Y (/Y++).

[0013] Next, the 1st example of automatic generation of the LSI test pattern program in EWS1 or a circuit tester 4 is explained using drawing 4. When the command of test pattern selection is given using input unit 5 grade to EWS1 or a circuit tester 4, first, EWS1 or a circuit tester 4 In step S41, the

information (especially class etc.) is extracted based on the part number of the semiconductor memory which it is going to examine, and the kind of information is used as a key. The CAD information (configuration information on memory and array information on a memory cell) about capacity, the number of I/O, etc. in a class of the semiconductor memory can be displayed on the screen of a display 6, and can be acquired. Under the present circumstances, naturally information, such as the class and capacity about the semiconductor memory which it is going to examine, and the number of I/O, can also be displayed on the screen of a display 6.

[0014] Therefore, in step S41, EWS1 or a circuit tester 4 reads the test-condition database about the kind (form) of the test objective memorized by storage 2 of a certain kind of semiconductor memory. By displaying on a display 6 the test-condition chart shown in drawing 3, a programmer The design CAD information that the kind of a certain kind which it is going to examine of capacity, the number of I/O, etc. in semiconductor memory are related to origin The test pattern number for every steps of a series of suitable for capacity, the number of I/O, etc. of the semiconductor memory which is going to carry out [ above-mentioned ] a trial out of the above-mentioned test-condition chart is chosen as shown in drawing 5, and it is stored temporarily at internal memory or storage 2. That is, it means that a test pattern 01 is chosen in step 1, and the test pattern 03 was chosen and stored temporarily in step 2. In addition, let the part which performs this pattern selection step S41 be the test-condition selection section.

[0015] Next, a programmer judges whether it is necessary to set up a test pattern option in step S42 based on the design information by which an indication was given [ above-mentioned ]. EWS1 or a circuit tester 4 may perform this decision automatically. As setting out of this test pattern option, a test pattern is not generated from a start address ( $X_s$ ,  $Y_s$ ), but it becomes setting out of the increment which occurs and can set the case where you want to generate a test pattern, in that case from the count increment or the address which carried out the decrement of the request from the intermediate address, i.e., a start address, or the count of a decrement. Moreover, as setting out of a test pattern option, from the fail bit map shown in drawing 11 (a) which is the test result of step 1 by which reading appearance is carried out from a circuit tester 4 - N, it may choose and the step number which gives OR operation may be set as drawing 7, as a RE point shows. Usually, all OR operation is given from the fail bit map shown in drawing 11 (a) which is the test result of step 1 by which reading appearance is carried out from a circuit tester 4 - N, and a total fail bit map is created. Thus, in step S42, when a test pattern option needs to be set up, setting out of a pattern option is performed in step S43.

[0016] When setting up an increment or the count of a decrement, it sets to EWS1 or a circuit tester 4. As the arrangement of the configuration of semiconductor memory, a memory cell, etc. based on the capacity of semiconductor memory and the number CAD information of I/O which it is going to examine is displayed on the screen of a display 6 and the chain line shows to drawing 6 The input units 5, such as a mouse, are used to this displayed semiconductor memory, for example, it is the greatest test area (a continuous line shows.). When setting up in a rectangle configuration (one-dimension is also included) etc. (the complicated configuration which has irregularity in addition to a rectangle configuration is sufficient although setting out becomes complicated somewhat), It becomes possible from the distance between the address ( $X_s$ ,  $Y_s$ ) of a starting point, and the address ( $X_i$ ,  $Y_i$ ) of an intermediate point to set up an increment or the count of a decrement. In addition, it is 2 bits or more two or more bits in X and the direction of Y as a unit of an increment or a decrement. In the case of 2 bits, it becomes every other line and every other bit. Moreover, when setting up the step number which gives OR operation, for example, the chart which described the test pattern name corresponding to the step number shown in drawing 7 is displayed on a display 6, and it is set up choosing so that it may be suitable for the target failure analysis, i.e., by performing control of a step (flow).

[0017] Next, step S44 is explained. Let the part which performs this step S44 be the scan field setting-out section. Namely, EWS1 or a circuit tester 4 displays on the screen of a display 6 the arrangement of the configuration of semiconductor memory, a memory cell, etc. based on CAD information about the kind of a certain kind which it is going to examine of the capacity and the number of I/O in semiconductor memory. As shown in drawing 6 , by setting up the greatest test area ( $W_x$ ,  $W_y$ ) in a

rectangle configuration (one dimension also being included) etc. to this displayed semiconductor memory, using the input units 5, such as a mouse It is inputted from a display 6 to EWS1 or a circuit tester 4 as X address and Y address ( $X_s, Y_s$ ) of a starting point of the test pattern 01 in step 1 when being chosen as selection of a test pattern is shown in drawing 5 (steps S441 and S442). It stores temporarily at an internal memory or storage 2. In addition, in the case of DRAM or SRAM, the greatest test area ( $W_x, W_y$ ) is about decided by capacity or the number of I/O. Therefore, in the case of DRAM or SRAM, EWS1 or a circuit tester 4 can compute the greatest test area ( $W_x, W_y$ ) automatically from the capacity of a test objective etc., and can also display it on the screen of a display 6.

[0018] Next, when the end point of the test pattern 01 in step 1 is in agreement with the greatest above-mentioned test area (a continuous line shows.), it can be found in the above-mentioned field setting out, and by inputting the address of this end point, EWS1 or a circuit tester 4 will ask for the count of an increment of the direction of X in the meantime, and the count of an increment of the direction of Y, and will store them temporarily at an internal memory or storage 2 (steps S443 and S444). moreover, when the end point of the test pattern 01 in step 1 comes to show in the greatest above-mentioned test area with the end point ( $X_e, Y_e$ ) of an alternate long and short dash line By inputting the address in the meantime by specifying the field of an alternate long and short dash line, EWS1 or a circuit tester 4 It will ask for the count of an increment of the direction of X in the meantime, and the count of an increment of the direction of Y, and will store temporarily at an internal memory or storage 2 (steps S443 and S444). In addition, as mentioned above, as a unit of an increment, it is also possible to make it two or more bits in X and the direction of Y.

[0019] The scan field of test pattern generating for every step by the above will be set up by the count of an increment or the count of a decrement of the address ( $X_s, Y_s$ ) of a starting point, the direction of X, and the direction of Y.

[0020] Since the class of test pattern for every steps of a series of was chosen and the scan field for test pattern generating for every step was determined in step S44 in step S41 as explained above In step S45, by reading to the step numerical order stored temporarily at an internal memory or storage 2, EWS1 or a circuit tester 4 generates a series of test pattern programs, as shown in drawing 8 . Let the part which performs this step S45 be the program generation section. First, the signal which followed the pattern at the start address ( $X_s, Y_s$ ) Write or read ("1" or "0") (step S451). [ for example, ] Next, according to a pattern (scanning pattern), an increment or a decrement is carried out for X address and Y address (step S452). Write the signal according to a pattern to the new address (X, Y) by this increment or decrement. Or a series of test pattern programs are generated by covering a series of step numbers chosen as shown in drawing 5 in between in the scanning zone to read (step S453) and where the address was set up in step S454, and repeating steps S452-S453. in addition -- although it will differ at this time as the starting point of the test pattern for every step is shown in drawing 2 -- the address ( $X_s, Y_s$ ) of the starting point of the scan field for test pattern generating -- and -- and since the point ( $X_e, Y_e$ ) is inputted, EWS1 or a circuit tester 4 can compute easily the count of an increment or the count of a decrement of the starting point of the test pattern for every step, the direction of X, and the direction of Y.

[0021] Next, the 2nd example of automatic generation of the LSI test pattern program in EWS1 or a circuit tester 4 is explained using drawing 9 and drawing 10 . The difference from the 1st example is in this 2nd example to have formed the capacity selection step S81 to the semiconductor memory which is a test objective. In the 1st example, by inputting the part number of the semiconductor memory to carry out which will examine capacity selection explained that it carried out automatically. Since the CAD information as a definition file to the capacity in a certain kind of semiconductor memory (for example, DRAM, SRAM, FLASH, etc.) is stored in the store 2 as a database in the case of the 2nd example EWS1 or a circuit tester 4 is this definition file (it is shown in drawing 10 ). Capacity selection is performed by reading from storage 2, displaying on a display 6, and specifying on a screen from the capacity of the semiconductor memory which a programmer is going to examine. In the condition of having doubled at capacity on the screen for setting up the scan field shown in drawing 6 , the CAD information in that capacity is displayed by this capacity selection, and setting out of a scan field becomes easy by it. Moreover, when it increases so that capacity may be 1M, 4M, and .., setting out of a

scale factor needs to be made to arbitration as a screen shown in drawing 6. That is because it is necessary to make it energy setting out by energy adjustment of the scan field by the high scale factor from rough setting out by the coarse control of the scan field in a low scale factor.

[0022] Next, fail bit map creation is explained. A series of test pattern programs generated by EWS1 or the circuit tester 4 in step S45 as mentioned above are written in the semiconductor memory 3 for circuit tester 4 blank test, and a circuit tester 4 reads the test result, and sets it in a circuit tester 4. Write in with a test result for every step number in the test judging section (not shown), compare per the expected value (reference value judged to be a fail bit) over a signal, and bit (cel), and pass / fail bit signal is generated. It changes into the address which is common for every step number in the address translation section (not shown), a step number 1 - N are covered, and it is a fail bit map (for example, it is shown in drawing 11 (a)) for every step number. It creates and memorizes to temporary memory. next, EWS1 or a circuit tester 4 from the fail bit map for every step number covering the step number 1 stored temporarily in the above-mentioned memory - N The fail bit map shown in drawing 11 (b) by making OR operation about the fail bit map of the step numbers 1, 3, and 4N shown with a RE point drawing 7 chosen by setting out of the pattern option shown at step S43 in drawing 4 and drawing 9 is created. It stores in the fail memory section (not shown).

[0023] Moreover, by carrying out OR operation about a fail bit map ranging from the fail bit map to all step numbers for every step number covering the step number 1 stored temporarily in the above-mentioned memory - N, EWS1 or a circuit tester 4 creates the fail bit map shown in drawing 11 (b), and its storing \*\*\*\*\* is also good for the fail memory section (not shown).

[0024] By the above, in EWS1 grade, the foreign matter and defect map data which are obtained from defective test equipment, such as foreign matter test equipment and a circuit pattern, through a network 7 can be compared with the fail bit map data stored in the above-mentioned fail memory section, and it is in location gap tolerance, and can ask for whenever [ coincidence ], whenever [ this coincidence / that was called for ] can be displayed on an indicating equipment 6, and the manufacture process factor which became a fail bit can be studied.

[0025]

[Effect of the Invention] The effectiveness it is ineffective to generating easily being possible is done so, without according to this invention, remaking a test pattern program extensively in semiconductor memory, such as DRAM, SRAM, and FLASH, even if capacity, the number of I/O, etc. are changed.

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[Translation done.]

## \* NOTICES \*

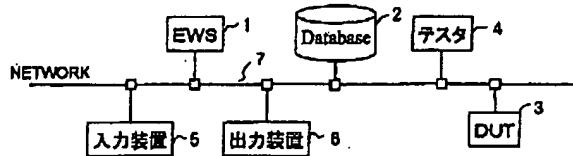
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## DRAWINGS

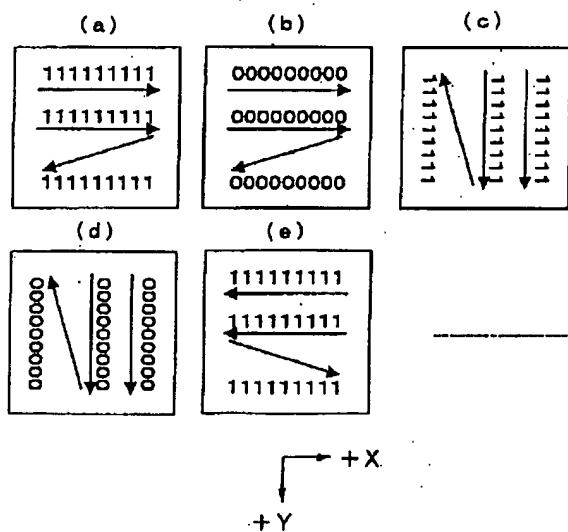
## [Drawing 1]

図 1



## [Drawing 2]

図 2



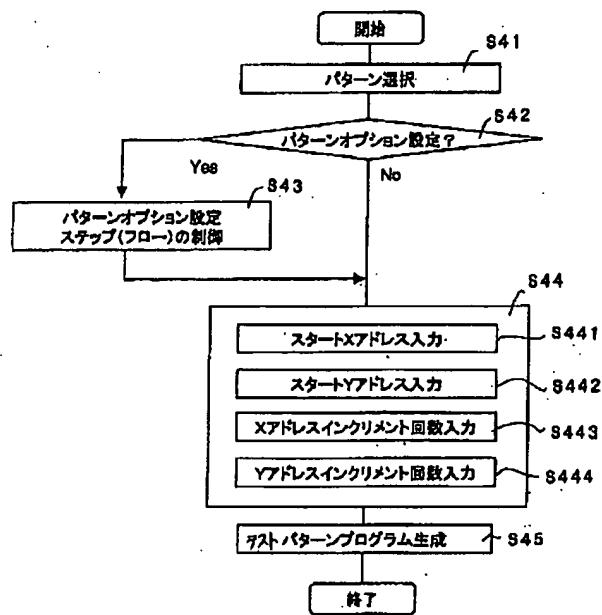
## [Drawing 3]

図 3

バタン名	走査型
PTN01	IWRITE X++/Y++
PTN02	OWRITE X++/Y++
PTN03	I READ/OWRITE X++/Y++

## [Drawing 4]

図 4



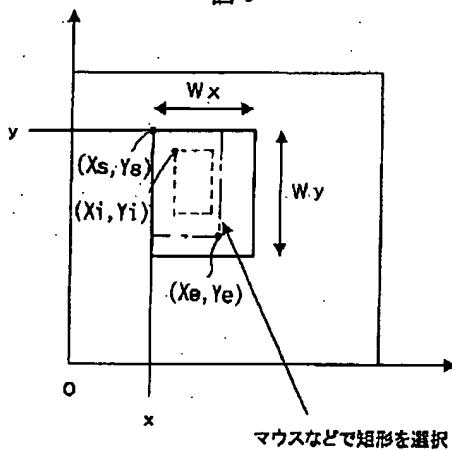
[Drawing 5]

図 5

ステップ	パターン名
1	PTN 01
2	PTN 03

[Drawing 6]

図 6



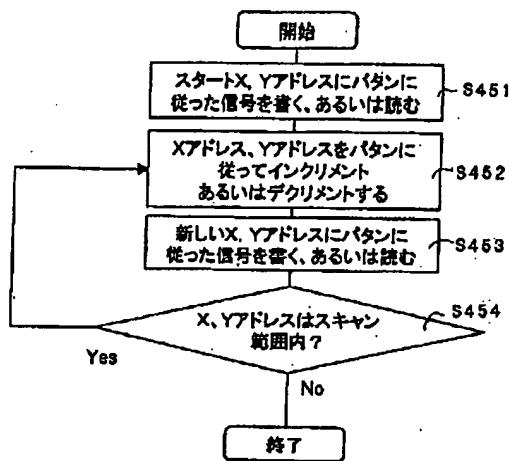
[Drawing 7]

図7

	ステップ	パターン名
✓	1	PTN1
	2	PTN3
✓	3	PTN4
✓	4	PTN6
	5	PTN2
✓	N	PTNn

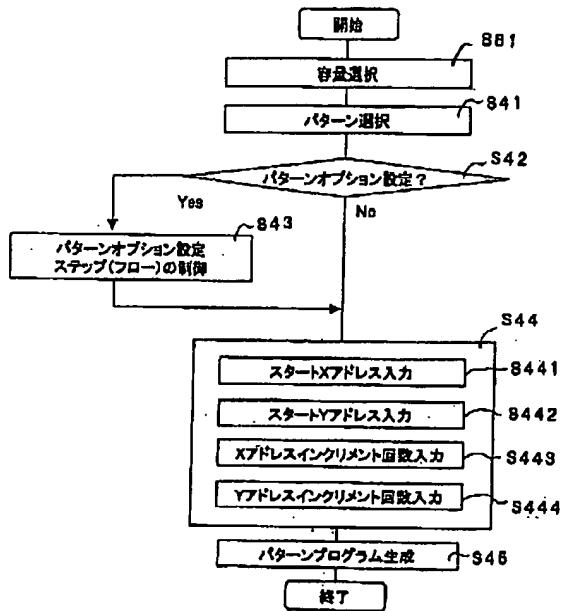
[Drawing 8]

図8



[Drawing 9]

図9



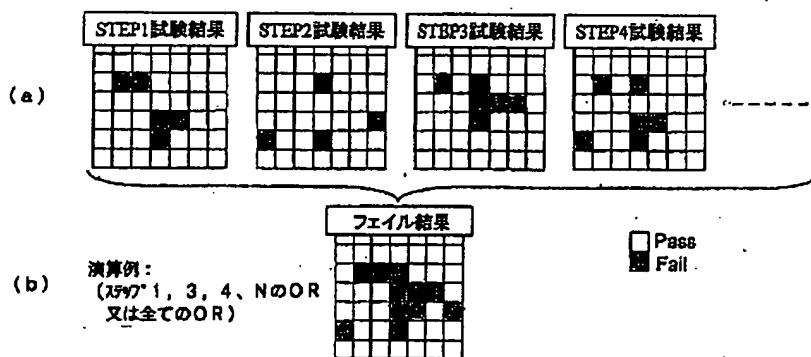
[Drawing 10]

図 10

容量	定義ファイル
64	MMM 1
256	MMM 8

[Drawing 11]

図 11




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[Translation done.]